UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,515	08/31/2001	Samuel H. Duncan	15311-2292	3331

24267   7590   03/05/2004

CESARI AND MCKENNA, LLP
88 BLACK FALCON AVENUE
BOSTON, MA 02210

EXAMINER
MASON, DONNA K

ART UNIT	PAPER NUMBER
2111	7

DATE MAILED: 03/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

		Application No	Applicant(s)
Office Action Summary		09/944,515	DUNCAN ET AL.
		Examiner	**Art Unit**
		Donna K. Mason	2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>23 December 2002</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-9 and 11-18</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-9 and 11-18</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>18 January 2002</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

U.S. Patent and Trademark Office

PTOL-326 (Rev. 1-04)   Office Action Summary   Part of Paper No./Mail Date 6

DETAILED ACTION

1.   Claims 1-9 and 11-18 are pending in this application. (It should be noted that

Applicant misnumbered the claims, skipping claim 10).

Specification

2.   The disclosure is objected to because of the following informalities:

On page 14, line 4, insert --be-- after "may".

Appropriate correction is required. See 37 CFR 1.71.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

4.   Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

5.   Claim 1 recites the limitation "the interrupt file" in line 18. There is insufficient

antecedent basis for this limitation in the claim. (For examination purposes, it should be

noted that claim 18 has been interpreted such that "at the interrupt file" in line 18 is

deleted).

6.   Claim 12 recites the limitation "the processor" in lines 10-11 and 12. There is

insufficient antecedent basis for this limitation in the claim. (For examination purposes,

it should be noted that claim 12 has been interpreted such that each occurrence of "the

processor" is replaced with --the at least one processor--).

7.   Claim 12 recites the limitation "a given port of the I/O bridge" in line 10. Applicant

should be careful to distinguish between "a given port of the I/O bridge" from the later

recited "interrupt port" in claim 13 (For examination purposes, claim 12 has been

interpreted such that "the given port of the I/O bridge" refers back to the previously

recited "plurality of ports" in line 6).

8.   Claim 16 recites the limitation "the serial shift register" in line 3. There is

insufficient antecedent basis for this limitation in the claim. (For examination purposes,

claim 16 has been interpreted such that "a parallel-load shift register" in line 2 is

replaced with --a parallel-load serial shift register-- and "the serial shift register" in line 3

is replaced with --the parallel-load serial shift register--).

9.   Applicant is advised to review each of the claims for similar antecedent basis

problems, in view of any corrections made in response to the above rejections.

10.   Claims 2-9, 11, 13-15 and 17-19 inherit the indefiniteness of independent claims

1 and 12.

Claim Rejections - 35 USC § 102

11.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12.   Claims 1-9 and 11-18 are rejected under 35 U.S.C. 102(e) as being anticipated

by U.S. Patent No. 5,956,516 to Pawlowski.

With regard to claims 1-8, Pawlowski discloses a method for preventing passive

release of interrupts within a computer system, the computer system having at least one

processor (Fig. 1, item 12) for servicing the interrupts, one or more input/output (I/O)

devices (Fig. 1, items 50, 52, 54, 56, and 58) configured to issue interrupts (column 3,

lines 24-26), and an I/O bridge (Fig. 1, item 12) having a plurality of ports (Fig. 1, item

38) to which I/O devices are coupled and configured to interface between the I/O

devices and the processor. The method includes the steps of: asserting an interrupt

signal by a subject I/O device coupled to a given port of the I/O bridge (column 3, lines

24-26); forwarding an interrupt message corresponding to the interrupt signal to the

processor for servicing (column 3, lines 50-53); setting an interrupt pending flag in

response to assertion of the interrupt signal (column 5, lines 45-49). In response to the

interrupt being serviced, generating a first ordered message, the first ordered message

notifying the subject I/O device that the interrupt has been serviced, and sending the

first ordered message to the given port of the I/O bridge (column 6, lines 40-41);

generating a second ordered message for clearing the interrupt pending flag, and

sending the second ordered message to the given port of the I/O bridge after the first

message has been sent (column 6, lines 44-45); deasserting the interrupt signal in

response to the first message (column 6, lines 49-50); and clearing the interrupt

pending flag at the interrupt file in response to the second ordered message (column 6, lines 40-41). With regard to the features of claims 2-8, see column 6, lines 37-65.

With regard to claim 9, Pawlowski discloses the method where the computer system includes a plurality of processors (column 3, lines 50-53), at least one of which is designated to service interrupts from the subject I/O device, and a plurality of I/O bridges (Fig. 1, items 16 and 82) each I/O bridge coupled to a plurality of I/O devices configured to assert respective interrupt signals.

With regard to claims 11 and 18, Pawlowski discloses the method and computer system where the interrupt signals are level sensitive interrupts (LSIs) (column 6, lines 21-36).

With regard to claim 12, Pawlowski discloses a computer system (Fig. 1, item 10) including: a plurality of input/output (I/O) devices (Fig. 1, items 50, 52, 54, 56, and 58) configured to assert and deassert respective interrupt signals (column 3, lines 24-26); at least one processor (Fig. 1, item 12) for servicing interrupts from the I/O devices; and an I/O bridge (Fig. 1, item 16) configured to interface between the I/O devices and the at least one processor, the I/O bridge having a plurality of ports (Fig. 1, item 38) to which the I/O devices are coupled and an interrupt controller (Fig. 1, item 34) configured to detect the assertion and deassertion of the interrupt signals. The interrupt controller, in response to assertion of an interrupt signal by a subject I/O device coupled to a given I/O bridge port, issues an interrupt message to the processor and sets an interrupt pending flag (column 5, lines 45-49). The processor, upon servicing the interrupt, sends first and second ordered messages to the given port of the I/O bridge, the first ordered

message notifying the subject I/O device that the interrupt has been serviced, and the

second ordered message clearing the interrupt pending flag (column 6, lines 37-48); the

subject I/O device deasserts the interrupt signal in response to the first message

(column 6, lines 49-50); and the interrupt pending flag is cleared in response to the

second ordered message (column 6, lines 40-41).

With regard to claims 13 and 14, Pawlowski discloses the computer system

where the I/O bridge further includes an interrupt port (Fig. 1, item 38) at which the

interrupt controller is disposed, and the given port of the I/O bridge forwards the second

ordered message to the interrupt port after forwarding the first ordered message to the

subject I/O device.   Pawlowski also discloses the computer system where the interrupt

port of the I/O bridge includes at least one register (Fig. 3, item 170) at which the

interrupt pending flag is implemented.

With regard to claim 15, Pawlowski discloses the computer system where the I/O

bridge port includes a read cache for buffering messages received from the at least one

processor, and an ordering engine operatively coupled to a read cache, and the

ordering engine is configured to release ordered messages buffered in the read cache

in the same order as which they were received (column 4, lines 56-60).

With regard to claims 16 and 17, Pawlowski discloses computer system, further

including an interrupt collector having a parallel-load shift register for receiving the

interrupt signals from the I/O devices, the serial shift register configured to transfer

information indicating the assertion or deassertion of interrupt signals to the interrupt

controller through one or more serial shift operations, and where the interrupt collector

transfers the information in response to a request from the interrupt controller, and the

interrupt controller is configured to limit the number of serial shift operations performed

by the interrupt collector so as to receive only information associated with interrupt

signals that have been enabled (see column 5, lines 41-64).

Therefore, Pawlowski reads on the invention as claimed.

13.   Claims 1, 12, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by

U.S. Patent No. 6,065,088 to Bronson, et al. ("Bronson").

With regard to claims 1 and 12, Bronson discloses a method and computer

system (Fig. 1) including: a plurality of input/output (I/O) devices (Fig. 1, items 90)

configured to assert and deassert respective interrupt signals; at least one processor

(Fig. 1, item 80) for servicing interrupts from the I/O devices; and an I/O bridge (Fig. 1,

item 70) configured to interface between the I/O devices and the at least one processor,

the I/O bridge having a plurality of ports (Fig. 1, item 113) to which the I/O devices are

coupled and an interrupt controller (Fig. 1, item 103) configured to detect the assertion

and deassertion of the interrupt signals. The interrupt controller, in response to

assertion of an interrupt signal by a subject I/O device coupled to a given I/O bridge

port, issues an interrupt message to the processor and sets an interrupt pending flag

(column 6, lines 38-41). The processor, upon servicing the interrupt, sends first and

second ordered messages to the given port of the I/O bridge, the first ordered message

notifying the subject I/O device that the interrupt has been serviced, and the second

ordered message clearing the interrupt pending flag (column 7, lines 2-10 and lines 48-

53); the subject I/O device deasserts the interrupt signal in response to the first

message (column 7, lines 9-10); and the interrupt pending flag is cleared in response to

the second ordered message (column 7, lines 9-10).

With regard to claim 15, Bronson discloses the computer system where the I/O

bridge port includes a read cache for buffering messages received from the at least one

processor, and an ordering engine operatively coupled to a read cache, and the

ordering engine is configured to release ordered messages buffered in the read cache

in the same order as which they were received (column 8, lines 57-67 to column 9, lines

1-16).

Therefore, Bronson reads on the invention as claimed.

Conclusion

14.   A shortened statutory period for reply is set to expire THREE MONTHS from the

mailing date of this communication. Extensions of time may be available under the

provisions of 37 CFR 1.136(a). In no event, however, will the statutory period for reply

expire later than SIX MONTHS from the mailing date of this communication.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Donna K. Mason whose telephone number is (703) 305-

1887. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mark H. Rinehart can be reached on (703) 305-4815. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM
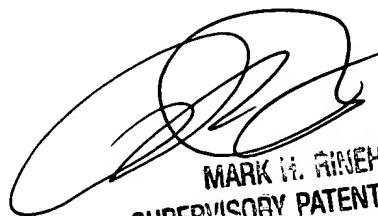
MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100